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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,630	01/25/2001	Hideo Miyake	1614.1116	5739

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,630	MIYAKE ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 have been considered. Claims 1-5 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment filed 01 May 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being taught by Saulsbury et al., U.S. Patent Number 6,314,510 (herein referred to as Saulsbury).

5. Referring to claim 1, Saulsbury has taught a computer which performs parallel processing of a plurality of programs in a time-division fashion, comprising:

a. A memory (Saulsbury column 2, lines 40-47 and Figure 1);

b. An instruction fetch unit configured to fetch instructions from said memory (Saulsbury column 2, lines 40-47 and Figure 1);

c. Hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs (Saulsbury column 1, lines 34-48; column 2, line 56 to column 3, line 38; Figure 1; and Figure 2);

d. An evacuation unit which records identification information identifying a first program, and evacuates information stored in an area of said plurality of areas if the area is necessary for execution of a second program and is being used for execution of the first program, said information being evacuated to a portion of said memory that corresponds to the first program (Saulsbury column 1, lines 34-48; column 2, line 54 to column 3, line 38; column 3, line 52 to column 4, line 9; Figure 1; and Figure 2); and

e. A restoration unit which restores the evacuated information to the area based on the identification information when the second program comes to a halt or to an end (Saulsbury column 4, lines 52-65 and Figure 4).

6. Referring to claim 2, Saulsbury has taught the computer as claimed in claim 1, further comprising an interruption unit which brings about interruption processing if the area is necessary for execution of a second program and is being used for execution of the first program, wherein said evacuation unit operates as part of the interruption processing to record the identification information and to evacuate the information stored in the area (Saulsbury column 1, lines15-22 and 34-48; column 2, line 54 to column 3, line 38; column 3, line 52 to column 4, line 9; Figure 1; and Figure 2) .

7. Referring to claim 3, Saulsbury has taught a computer which performs parallel processing of a plurality of programs in a time-division fashion, comprising:

a. A memory (Saulsbury column 2, lines 40-47 and Figure 1);

b. An instruction fetch unit configured to fetch instructions from said memory (Saulsbury column 2, lines 40-47 and Figure 1);

c. Hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs (Saulsbury column 1, lines 34-48; column 2, line 56 to column 3, line 38; Figure 1; and Figure 2);

d. An evacuation unit which records identification information identifying a first program, and evacuates information stored in a first area of said plurality of areas if the first area and a second area of said plurality of areas are necessary for execution of a second program and are being used for execution of the first program, said evacuation unit subsequently evacuating information stored in the second area when use of the second area becomes actually necessary for execution of the second program, said information being evacuated to a portion of said memory that corresponds to the first program (Saulsbury column 1, lines 34-48; column 2, line 54 to column 3, line 38; column 3, line 52 to column 4, line 9; Figure 1; and Figure 2); and

e. A restoration unit which restores the evacuated information to the first and second areas based on the identification information when the second program comes to a halt or to an end (Saulsbury column 4, lines 52-65 and Figure 4).

8. Referring to claim 4, Saulsbury has taught a method of controlling a computer which performs parallel processing of a plurality of programs in a time-division fashion, said computer having a memory and an instruction fetch unit configured to fetch instructions from said memory, comprising:

a. Providing hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs (Saulsbury column 1,

lines 34-48; column 2, line 56 to column 3, line 38; Figure 1; and Figure 2);

b. Recording identification information identifying a first program, and evacuating information stored in an area of said plurality of areas if the area is necessary for execution of a second program and is being used for execution of the first program, said information being evacuated to a portion of said memory that corresponds to the first program (Saulsbury column 1, lines 34-48; column 2, line 54 to column 3, line 38; column 3, line 52 to column 4, line 9; Figure 1; and Figure 2); and

c. Restoring the evacuated information to the area based on the identification information when the second program comes to a halt or to an end (Saulsbury column 4, lines 52-65 and Figure 4).

9. Referring to claim 5, Saulsbury has taught a method of controlling a computer which performs parallel processing of a plurality of programs in a time-division fashion, said computer having a memory and an instruction fetch unit configured to fetch instructions from said memory, comprising:

a. Providing hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs (Saulsbury column 1, lines 34-48; column 2, line 56 to column 3, line 38; Figure 1; and Figure 2);

b. Recording identification information identifying a first program, and evacuating information stored in a first area of said plurality of areas if the first area and a second area of said plurality of areas are necessary for execution of a second program and are being used for execution of the first program, followed by

subsequently evacuating information stored in the second area when use of the second area becomes actually necessary for execution of the second program, said information being evacuated to a portion of said memory that corresponds to the first program (Saulsbury column 1, lines 34-48; column 2, line 54 to column 3, line 38; column 3, line 52 to column 4, line 9; Figure 1; and Figure 2); and

c. Restoring the evacuated information to the first and second areas based on the identification information when the second program comes to a halt or to an end (Saulsbury column 4, lines 52-65 and Figure 4).

10. Claims 6-7 are rejected under 35 U.S.C. 102(e) as being taught by Gottlieb, U.S. Patent Number 6,298,431 (herein referred to as Gottlieb).

11. Referring to claims 6 and 7, taking claim 6 as exemplary, Gottlieb has taught a computer for parallel processing, comprising

a. An evacuation unit which records identification information identifying a first program stored in one of a plurality of areas of a hardware resource being used in parallel by at least two of a plurality of programs, if the area is necessary for execution of a second program, and evacuates the information (Gottlieb column 2, lines 47-62; column 3, lines 39-46; column 4, lines 19-60; column 5, line 24 to column 6, line 9; column 7, line 52 to column 8, line 11; Figure 1; and Figure 2). In regards to Gottlieb, the identification information is inherent to the banked shadow registers, since some sort of identification is necessary for the system to correctly identify which thread information must be loaded on a thread switch.

b. A restoration unit which restores the evacuated information to the area based on

the identification information when the second program comes to a halt or to an end (Gottlieb column 2, lines 47-62; column 3, lines 39-46; column 4, lines 19-60; column 5, line 24 to column 6, line 9; column 7, line 52 to column 8, line 11; Figure 1; and Figure 2).

12. Claim 7 is substantially similar in function to claim 6 and rejected for the same reasons set forth above. The only difference in claim 7 is a method claim and claim 6 is an apparatus claim.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Referring to claim 8, Gottlieb has taught a computer which performs parallel processing of a plurality of programs in a time-division fashion, comprising:

a. Evacuating information associated with an executing first program and identified by a first program identifier where the information is located in a first area of a processor and is evacuated when the area is necessary for execution of a second program (Gottlieb column 2, lines 47-62; column 3, lines 39-46; column 4, lines 19-60; column 5, line 24 to column 6, line 9; column 7, line 52 to column 8, line 11; Figure 1; and Figure 2). In regards to Gottlieb, the identification information is inherent to the banked shadow registers, since some sort of identification is

necessary for the system to correctly identify which thread information must be loaded on a thread switch.

b. Restoring the evacuated information to the first area using the identifier when the second program ends execution (Gottlieb column 2, lines 47-62; column 3, lines 39-46; column 4, lines 19-60; column 5, line 24 to column 6, line 9; column 7, line 52 to column 8, line 11; Figure 1; and Figure 2).

2. Gottlieb has not taught said information being evacuated outside said computer. Handy has taught said information being evacuated outside said computer (Handy pages 62-64). A person of ordinary skill in the art at the time the invention was made, and as taught by Handy, copying data from local memory, in Handy's case a cache, to main memory only when needed, e.g. when local memory is full, reduces the amounts of time the main memory is accessed, thereby reducing the amount of time the main memory bus is and processor speed is increased (Handy page 63, paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the copying method of Handy in the device of Gottlieb to increase processor speed.

Response to Arguments

14. Examiner withdraws the drawing objections in favor of the claim amendments.

15. Examiner withdraws the previous 35 U.S.C. §112, first paragraph, rejections with regards to claims 1, 3, 4, and 5 in favor of the amendments.

16. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

17. Applicant's arguments filed 01 May 2006 have been fully considered but they are not persuasive.

18. Applicant argues in essence on pages 5-7, with regards to claims 6-7, "Gottlieb neither teaches, discloses, nor suggests, 'a hardware resource being used in *parallel* by at least two of a plurality of programs,'...". This has not been found persuasive. Applicant's arguments suggest that the claim language means that one hardware resource is being used by at least two programs at once. However, the Examiner could not locate support for this argument within the specification and it is unclear how a hardware resource can be used in such a manner. A single hardware resource cannot be accessed by multiple programs simultaneously, as suggested by the arguments, since this type of access would cause data corruption and execution errors. Should the claim language be interpreted in this manner, there would be a lack of support in the specification, since the specification describes "a hardware resource being used in parallel" as a resource that has context data in a hardware resource of one incomplete program being saved to memory on a context switch so that another incomplete process may run and use the resource, see Figures 16 and 17 of Applicant's own specification for examples, not that both programs use a hardware resource at the same time. The Examiner maintains her rejection based upon the interpretation of "a hardware resource being used in parallel" consistent with the specification.

19. Applicant's argue in essence on page 9 with regards to claim 8

> Gottlieb neither teaches, discloses, nor suggests, 'evacuated to outside the processor'...
>
> ...modifying Gottlieb as proposed in as proposed in the Office Action would also change the principal of operation of Gottlieb...

20. This has not been found persuasive. The intended modification was not to replace the shadow register file, but that when the shadow register file is full, the data would be evacuated to main memory, which is outside of the processor. As the Examiner stated in her reasons for combining "A person of ordinary skill in the art at the time the invention was made, and as taught by Handy, copying data from local memory, in Handy's case a cache, to main memory only when needed, e.g. **when local memory is full**..." The Examiner meant the combination for when the backing register, which stores information for other threads and contexts, is full and cannot save the current context/thread needed to be stored, then main memory must be utilized to store the overflow of information, e.g. information associated with a first program is evacuated outside of the processor to main memory when the area for a second program to be stored there during another context switch.

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
19 July 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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